Self-assembly of metallic double-dot single-electron device

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We present an approach that allows forming a nanometric double dot single electron device. It uses chemical synthesis of metallic nanoparticles to form dimeric structures, e-beam lithography to define electrodes and gates, and electrostatic trapping to place the dimers in between the electrodes. We demonstrate a control of its charge configuration and conductance properties over a wide range of external voltages. This approach can be straightforwardly generalized to other material systems and may allow realizing quantum information devices. © 2011 American Institute of Physics. [doi:10.1063/1.3624899]

Single electron devices are a subject of large current interest because of their potential applications as nanometric transistors, memory elements, and quantum information devices.^{1,2} Acquiring non-trivial functionality with such devices requires complex structures that combine together a few coupled domains. This challenge was addressed in semiconductor nanostructures, mainly by implementing advanced lithography on two-3-5 or one-6-8 dimensional structures. However, realizing such devices in metals, where a wealth of new effects and applications can be realized,⁹ is challenging, as the tunnel barriers have to be sub-nanometric in width. This requirement practically excludes the use of lithography as a mean for constructing a metallic multi-dot nanometric device and calls for a different approach. Experimental attempts to address this challenge have been reported.^{10,11}

In this work, we present a hybrid approach, which uses chemical synthesis of metallic nanoparticles (NPs) to form dimeric structures, electron beam lithography to define electrodes and gates, and electrostatic trapping to place the dimers in between the electrodes. This approach was first demonstrated¹² in measuring the conductance of a single dithiolated organic molecule. Here, we take this approach one step further and construct a full single electron device, in which the electrostatic potential on each of the NPs is controlled by a separate gate, and the tunnel barriers are predefined by the NPs capping layer. The device was operated in a wide range of external voltages resulting in more than 250 charge configurations of the dimer. This rich behavior provides an attractive arena for double dot physics research.

The device structure can be seen in Fig. 1(a). It consists of a dimer, made of two 17 nm NPs, connected in series to two gold leads (L & R). Four side gates, which are located \sim 50 nm from the dimer, allow control of the electrostatic potential on the dimer. Each couple of side gates, G1 and G2, acts differentially on the dimer, such that G1 affects predominantly the left NP and G2 the right NP. The measured ratio between the gate capacitance to the adjacent NP and the capacitance to the further NP is approximately 4, implying a good selectivity of the gates. This electrode's pattern sit on top of a 100 nm insulating SiO_2 layer, which is deposited on n-doped silicon substrate, that serves as a back-gate (BG).

The dimer consists of two gold NPs, which are covalently bonded by one or more linker molecules, 4,4'-biphenyldithiol (BPD). The process of dimerization requires the NPs to overcome their electrostatic repulsion and get to a distance of ~ 1 nm from each other. This can be achieved by gradually adding NaCl ions, which screen the repulsive forces between the negatively charged NPs and allow them to get close enough such that BPD mediated dimerization can take place. We found that ionic ligands, such as citrate, are incompatible with this process, and dimers formation with this ligand is hard to control: it requires delicate adjustment of the NP concentration. On the other hand, robust control of the dimerization is achieved with NPs covered by covalently bonded ligands. The strong repulsion between these NPs and the stability of the capping layer, allow dimerization through gradual addition of electrolytes. We have studied two such ligands, 3-mercaptobenzoic acid and



FIG. 1. (Color online) (a) Scanning electron microscope image of the double-dot device. The dimer, which is composed of 17 nm NPs, is aligned in series with the lead electrodes (L and R). (b) A sketch of the dimer and leads region, showing the capping layers and the linker molecule. (c) Gel matrix loaded with 34 nm NPs' solution that includes the linker molecule (right) and a corresponding control (left).

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mercaptosuccinic acid (MSA), and both allowed dimer formation with high yield. The capping layer forms a tunnel barrier for electrical conductance between the NP and the adjacent electrode or NP. We found that the conductance of the MSA-capped dimers was significantly higher (\sim 1 order of magnitude), and the results reported in this work are therefore of MSA-capped dimers. The inter-NPs and the NPelectrodes conductance were found to be of similar value (as will be shown later) and strongly dependent on the NP diameter: \sim 1 and \sim 100 nS for 17 and 34 nm, respectively. This shows that in the sub 100 mV drain-source voltage range, which is relevant for this work, the dimer conductance is mainly determined by the MSA capping layer and not by the linker molecule.

The dimerization process¹³ yields a solution which consists of single NPs and dimers. Using gel electrophoresis, we separate the dimers and extract them to a final solution containing $\sim 100\%$ (Ref. 13) BPD linked dimers (Fig. 1(c)). The dimers are brought to contact with the electrodes using electrostatic trapping. We apply an ac voltage of 1 V at 10 MHz for 60 s on the L and R electrodes that are covered with a droplet of the dimers' solution. The electrodes design is planned to form an electrostatic trap in which the dimers are aligned along the L-R axis in their final position. The trapping parameters were chosen such that $\sim 10\%$ of the devices (one out of eleven on a chip, which are simultaneously biased) had one trapped dimer. Atomic force microscopy (AFM) is then used to image the devices and select the ones that appropriately bridge the electrodes (typically, one of three dimers). The overall yield of the electrostatic trapping process is therefore approximately one measurable dimer for each three chips, which took 3 min to trap. These devices were cooled down to 4.2 K in a He refrigerator, and their conductance was measured.

Figure 2(a) shows the conductance through the dimer as a function of the gate voltages V_{G1} and V_{G2} at zero applied voltage between the left and right electrodes. It is seen that the conductance peaks are organized in a hexagonal structure, outlined by dashed lines. This honeycomb structure is well known for double dot systems:¹⁴ each of the domains that are delineated by the diagram is characterized by a different charge configuration (n_1, n_2) of the dimer (where n_1 , n_2 denote the number of electrons on NP₁, NP₂). We see that each conductance peak appears at the intersection of three domains and manifests the degeneracy of three charge configurations. At these points that are called *triple points*, the electrochemical potentials of the two dots (μ_1 and μ_2) and the leads (μ_L and μ_R) are aligned and current can flow. Figure 2(b) shows the behavior of the system at a larger gate voltage range, ± 4 V on each of the gates (G1,2). The figure represents more than 250 different charge configurations that can be realized, in which the charge on each of the dots can be changed by up to 18 electrons. A periodic pattern, with a period of 5 charge states, can be observed. This pattern was not seen with the 34 nm NPs that were prepared by a different method¹³ and is probably related to an internal structure of the 17 nm NPs.

To obtain a quantitative insight into the conductance properties of the system, we need to determine the capacitances and tunneling resistances of the various elements. The measurement in the $V_{G1} - V_{G2}$ plane can provide global information and some of the ratios between the capacitances but does not provide information on the coupling to the leads. This can be straightforwardly achieved by studying the conductance dependence on the applied voltage between the L and R electrodes, V_{SD} , in a back-gate configuration. The conductance in the $V_{BG} - V_{SD}$ plane is related to the honeycomb diagram in the $V_{G1} - V_{G2}$ plane: the V_{BG} axis is a cut in that diagram for which $V_{G1} = V_{G2}$, and V_{SD} is orthogonal to that plane. A result of such measurement is plotted in Fig. 3(a). Unlike the well known simple diamond-like structure, which is characteristic to a single dot behavior, here we observe a more complex structure, consisting of large and small blockade regions. The dashed lines in Fig. 3(a) manifest various possible alignments of the system's electrochemical potentials. The two diagonal ones manifest the alignment of the electrochemical potential of each NP with its close-by lead, $\mu_L = \mu_1(n_1 + 1, n_2)$ and $\mu_2(n_1, n_2) = \mu_R$. The third, which is parallel to the V_{BG} axis, manifests an alignment between the electrochemical potentials of the two NPs, $\mu_1(n_1, n_2) = \mu_2(n_1 - 1, n_2 + 1).$

The current through the system can be written² as the difference between the forward and backward tunneling rates at each of the three tunnel barriers in the system: $I = |e| \sum_{(n_1,n_2)} P(n_1,n_2) \{\Gamma_i^+(n_1,n_2) - \Gamma_i^-(n_1,n_2)\}$. Here, *e* is the electron charge and $P(n_1, n_2)$ is the probability to find the system in (n_1, n_2) charge configuration, and Γ_i^{\pm} are the forward and backward tunneling rates.^{2,15} Using the Nelder-Mead simplex find method,¹⁶ we looked for the system's six parameters (three capacitances and three tunneling resistances) that best correspond to the measured result. Figure 3(b) shows the calculated conductance that best fit the measured result of Fig. 3(a). The excellent correspondence between the two ($R^2 \sim 0.97$) confirms that the system is well described by this model. We have studied the influence of the cross capacitance terms (the capacitance between the left lead and NP₂)



FIG. 2. (Color online) (a) The measured conductance (in nS) of the device seen in Fig. 1(a) as a function of V_{G1} and V_{G2} . The dashed white lines separate domains with different charge configuration (n_1, n_2) . (b) A zoom out showing the behavior on a broader gate voltage range, ± 4 V, in which more than 250 different charge configurations are realized.

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FIG. 3. (Color online) (a) The measured conductance (in nS) of a device, based on 34 nm NPs, as a function of V_{BG} and V_{SD} . The high conductance regions, emphasized by the dashed lines, manifest various possible alignments of the electrochemical potentials $\mu_{1,2}$, $\mu_{L,R}$. (b) The calculated conductance using parameters, which best fit the measured result in (a): $C_{L1} = 6.9$ aF, $C_{12} = 9.5$ aF, $C_{2R} = 6.8$ aF, $R_{L1}^{-1} = 111$ nS, $R_{12}^{-1} = 240$ nS, and $R_{2R}^{-1} = 21$ nS.

and the right lead and NP_1) and found it to be an order of magnitude lower than the direct terms.

The model enables us to accurately extract the device parameters and thereby examine the reproducibility of the fabrication method. To this end, we studied a set of 12 devices, consisting of 34 nm particles. The mean value for the lead-NP capacitance is 8.0 ± 1.8 aF and for the inter NP capacitance -7.9 ± 1.4 aF. This distribution is impressively narrow, representing a good control of the electrodes and dimer parameters. On the other hand, the conductance values exhibit a broader distribution: the mean lead-NP conductance is 60 ± 48 nS and the inter-NP conductance 86 ± 74 nS. This can be partially explained by the trapping procedure, which is not fully reproducible, but probably reflects also variability in the capping layer conductance.

In summary, we demonstrated a technique to form a nanometric sized double dot system with control of its governing parameters. The technique can be straightforwardly generalized to other materials, in particular, semiconducting quantum dots, and may allow realizing quantum information and other single-electron devices.

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